High-quality silicon on silicon nitride integrated optical platform with an octave-spanning adiabatic interlayer coupler

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Abstract: Hybrid nanophotonic platforms based on three-dimensional integration of different photonic materials are emerging as promising ecosystems for the optoelectronic device fabrication. In order to benefit from key features of both silicon (Si) and silicon nitride (SiN) on a single chip, we have developed a wafer-scale hybrid photonic platform based on the integration of a thin crystalline Si layer on top of a thin SiN layer with an ultra-thin oxide buffer layer. A complete optical path in the hybrid platform is demonstrated by coupling light back and forth between nanophotonic devices in Si and SiN layers. Using an adiabatic tapered coupling method, a record-low interlayer coupling-loss of 0.02 dB is achieved at 1550 nm telecommunication wavelength window. We also demonstrate high-Q resonators on the hybrid material platform with intrinsic Q's as high as 3×10^6 for a 60 μm-radius microring resonator, which is (to the best of our knowledge) the highest Q observed for a micro-resonator on a hybrid Si/SiN platform.

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OCIS codes: (130.0130) Integrated optics; (230.5750) Resonators.

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1. Introduction

Since its advent in 1990s [1, 2], the success of silicon photonics has been critically hinged upon its compatibility with electronic device fabrication processes. Platforms based on silicon (Si) have been increasingly used in conjunction with CMOS fabrication processes to form a large set of integrated photonic devices and systems. Due to the high refractive index of Si and the resulting high optical confinement, photonic devices with submicron features have been successfully demonstrated for generation [3], high-speed manipulation [4–8] and detection of optical signals [9] in Si-based platforms. However, the intrinsic optical loss in Si (due to the free-carrier absorption (FCA) and the two-photon absorption (TPA)) limits its capability in handling high-power signals and supporting ultra-low-loss photonic devices. To

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address these shortcomings, various materials have been investigated which outperform Si in some of the key optical features (such as linear and nonlinear losses). Among alternatives, silicon nitride (SiN) is a promising platform for integrated photonic applications while being fully compatible with standard CMOS fabrication processes. Thin films of SiN, grown by high-temperature, low-pressure chemical vapor deposition (LPCVD), demonstrate ultra-low bulk absorption considerably lower than that of Si in near-infrared (near-IR) and a wide transparency window that extends into the visible range [10]. Recent studies on LPCVD SiN confirm 1-2 orders of magnitude lower optical loss compared to Si at near-IR wavelengths [11]. A reasonably high refractive index contrast with the substrate silicon oxide (SiO_2) layer allows tight confinement of the optical mode while reducing the loss due to fabrication imperfections such as the sidewall roughness. Also, its small nonlinear losses (e.g., TPA), high Kerr-nonlinearity figure-of-merit, and low dispersion enable a broad set of applications such as frequency comb [12] and supercontinuum generation over a wider range of optical spectrum (from near-IR to visible wavelengths).

In spite of such benefits, SiN lacks some of the key material characteristics required for optoelectronic devices (e.g., lack of a reliable tuning or high-speed modulation mechanism) due to its dielectric nature. One solution to resolve this issue is to develop a hybrid Si/SiN material platform, in which, different devices can be fabricated in different material layers based on the desired functionalities. Recently, two different approaches for integration of Si and SiN based on 1) the vertical integration of SiN on top of Si [13], and 2) back-end integration of SiN beneath Si [14] have been proposed. In the first approach, after processing the Si device layer of a silicon-on-isolator (SOI) substrate, the SiN layer is deposited on top of the Si layer (using high-temperature LPCVD), patterned, and annealed at 1100°C in N_2/O_2 ambient to minimize the material loss. The high-temperature nature of the fabrication sequence makes the process prone to dopant diffusion. Therefore the process is not CMOS-compatible. Also, the additional oxygen annealing oxidizes the active Si layer uncontrollably and changes the electronic and optical characteristics of the designed devices. Alternatively, the second approach uses a bonding process to transfer a layer of Si on top of a patterned SiN layer after planarization of the sample. While the second approach resolves the issue of high-temperature fabrication process, the reported devices to-date have been based on using a relatively thick (e.g., 600 nm) SiO_2 interface layer. Such thick buffer layers result in weak coupling of the photonic devices in different layers and impose long interlayer couplers (to couple light efficiently between Si and SiN layers) for low-loss applications. For example, an efficient interlayer coupler in such a platform can be 0.3 mm long [14]. On the other hand, such hybrid platforms are only demonstrated for thin SiN layers (40-100 nm) with low light confinement that does not support compact photonic devices. As an example, to achieve a resonator with a high intrinsic quality factor ($Q_{int} = 8 \times 10^7$), a ring resonator with the footprint of 20 mm × 20 mm is needed [15], while a ring of 1 mm × 1 mm area does not effectively confine light due to high radiation losses. As the result, such platforms are not suitable for dense integration of optoelectronic devices.

In this work, we present a new Si-on-SiN (SON) hybrid material and device platform in which a monolithic crystalline Si (c-Si) layer is integrated on an underlying SiN layer with a thin (i.e., 60 nm) SiO_2 interface layer. Using this platform, we demonstrate a hybrid tapered coupler with interlayer coupling losses as low as 0.02 dB and 30 μm total length. We also demonstrate high-Q (~3×10^6 intrinsic for 60 μm radius) SiN ring resonators on the SON platform, which is the same as the Q of the inspection resonators on the SiN-on-SiO_2 material platform, indicating high quality of the bonding process with a thin oxide interface layer. In contrast to previously reported methods, our proposed approach covers the entire device fabrication after the development of the hybrid material platform at the wafer-scale, making the platform formation and the device fabrication entirely separate from one another. This considerably reduces the complexity of the fabrication process and eliminates the need for the chemical-mechanical polishing (CMP) process.

In the rest of this paper, we present a detailed description of our platform fabrication process (Section 2), discuss the theoretical background and simulation of our coupler design

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(Section 3), and present the fabrication flow and characterization results of the fabricated devices (Section 4). Final conclusions are discussed in Section 5.

2.1 atform fabrication

Figure 1 shows an overview of our fabrication process. In this work, we envision a method that decouples the material platform development from the device fabrication, and therefore is fully compatible with wafer-scale processing. Here the process is done at the chip-scale using smaller wafer pieces (e.g. 2" by 2") for simplicity. The fabrication begins with two wafers (or pieces): an SOI wafer (from SOITEC) and a bare Si wafer. The SOI piece, piece 1 in Fig. 1(a), is first thinned down to the desired Si layer thickness (~230 nm) by thermal oxidation and wet etching of the oxide (Fig. 1(b)). The thinned Si layer is then thermally oxidized to achieve a 30 nm SiO_2 layer on a 220 nm crystalline Si film (Fig. 1(c)). The thickness of the Si device layer is chosen at 220 nm throughout this work to guarantee the single mode operation of Si waveguides. The bare Si piece, piece 2 in Fig. 1(d), is first thermally oxidized to grow 5 μm of SiO_2. In the next step, 400 nm of stoichiometric SiN is deposited by LPCVD (using a Tystar silicon nitride deposition furnace) at 800°C with dichlorosilane (DCS) and ammonia (NH_3) precursors at 1:3 gas ratio. The piece is further annealed at 1100°C to improve the quality of the SiN layer.

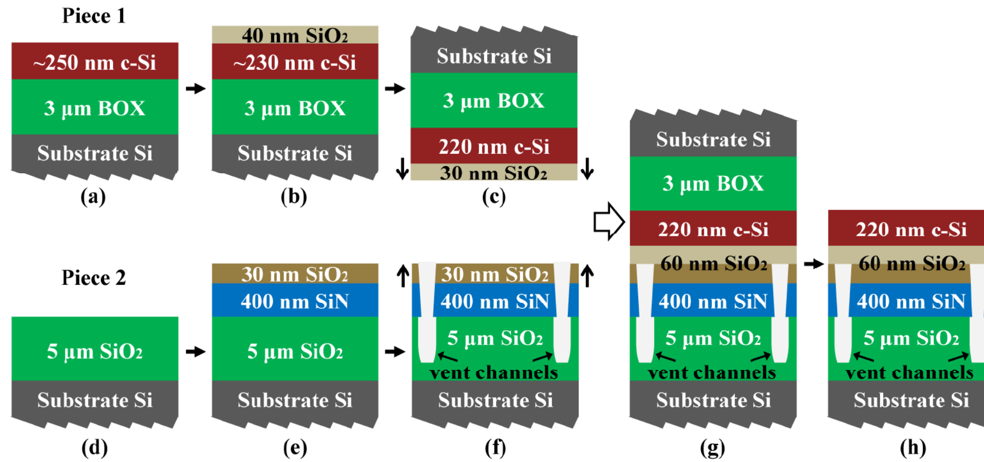

Fig. 1. Summary of the SON platform fabrication process. (a) Piece 1, an SOI piece. (b) Dry thermal oxidation reduces the Si thickness. (c) Wet etching of SiO_2 followed by the second dry oxidation. (d) Piece 2, a bare Si piece, goes through oxidation to grow 5 μm of SiO_2. (e) An LPCVD SiN layer is deposited, followed by the deposition of a 30-nm SiO_2 layer using ALD. (f) Vent channels are introduced using optical lithography, dry etching of SiN, and wet etching of bottom SiO_2 layer. (g) Two pieces are bonded using a low-temperature hydrophilic bonding method. (h) Backside removal of the Si substrate followed by wet etching of the BOX layer.

To deposit a thin layer of SiO_2 on SiN (Fig. 1(e)), we first test three different oxide deposition methods based on: 1) plasma-enhanced chemical vapor deposition (PECVD), 2) atomic layer deposition (ALD), and 3) hydrogen silsesquioxane (HSQ) spin coating. Since HSQ has to be annealed in the N_2 ambient to convert to SiO_2, all three samples were annealed at 800°C for 3 hours after deposition. The optical and mechanical quality of the resulting oxide layers were then compared based on two figures of merit: 1) surface roughness, and 2) SiN/SiO_2 interface bond strength. The first parameter was extracted using atomic force microscopy (AFM), and the results are shown in Fig. 2. The lowest average surface roughness (R_a) was obtained with HSQ annealing (R_a = 0.239 nm), while ALD (R_a = 0.383 nm) performing better than PECVD (R_a = 0.745 nm). The second parameter was measured by performing hydrophilic bonding on a pair of SiN on Si pieces with a thin (e.g., 30 nm) SiO_2 layer followed by the blade-crack-opening test, which is a simplified version of the wedge-opening test [16]. The crack depth was measured to be 2.1 mm for the annealed HSQ sample,

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while being less than 1 mm for the ALD sample. The result confirms that ALD oxide establishes stronger SiN/SiO_2 and SiO_2/SiO_2 bonding interfaces than the HSQ oxide. Therefore, ALD is chosen as the thin oxide deposition method due to its strong interface bond with the underneath SiN layer and a smooth interface layer, which is critically important for atomic-level bonding. In addition, ALD is the most precise method for deposition of a thin oxide layer with a desired thickness.

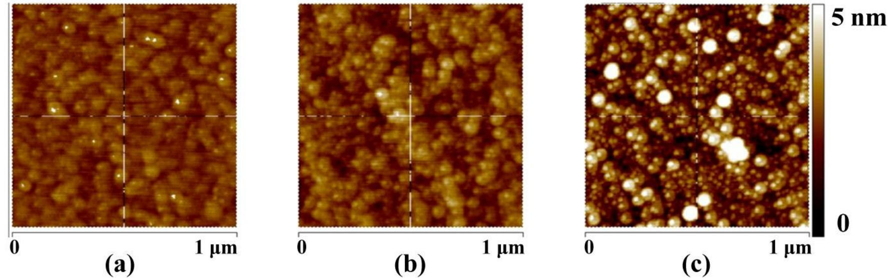

Fig. 2. AFM images from the surface of a 30-nm SiO_2 layer on SiN, deposited by (a) HSQ annealing, average surface roughness (R_a) is 2.39 Å; (b) ALD, R_a = 3.83 Å; (c) PECVD, R_a = 7.45 Å.

In the next step, a bonding technique is employed to fuse two pieces into one (Fig. 1(g)). Hydrophilic fusion bonding is a well-studied and widely-used technique to integrate different substrates into a monolithic piece. It has been used for various applications in micro- and nano-electromechanical system design and fabrication as well as integrated photonics [17–19]. In this work we used a low-temperature method that has been utilized to build the double-layer crystalline Si platform [20, 21]. The low-temperature nature of this technique is of particular interest for further electronic integration. However, when the thickness of the interface oxide is reduced below 200 nm, the quality and the yield of the low-temperature bonding drops [22]. SiO_2 is a fairly porous material, which can adsorb and transfer trapped/byproduct gases away from the interface. As the thickness of the SiO_2 is reduced, its corresponding out-gassing capacity reduces too, resulting in an increased number of voids formed at the interface. To reduce the number of these voids, we have included a set of horizontal vent channels that are spaced 250 μm apart. As illustrated in Fig. 3(a), these channels provide an exit path for trapped air and bonding byproducts to improve the quality of the interface bond. The introduction of vent channels enables void-free bonded interfaces and increases the total yield to close to 100% over the chip for oxide thicknesses as low as 30 nm (Fig. 3(b)). It also reduces the mechanical stress in the SiN layer, which allows the wafer-scale bonding.

Channels are added into the piece 2 after the thin ALD oxide is deposited on the SiN layer (Fig. 1(f)). First, a layer of 1813 photoresist is patterned using UV (365nm) lithography. Then, the SiO_2 and SiN layers are etched using reactive ion etching (RIE). In the next step, the piece is immersed in buffered oxide etchant (BOE) to remove 1 μm of the BOX layer at the bottom of the channels (Fig. 3(b)). Finally, the photoresist is stripped away and both pieces go through the hydrophilic bonding process, which is described in detail in [20]. After bonding the two pieces, the backside substrate of the SOI piece is removed using wet and/or dry etching of Si, in which the SiO_2 layer acts as the etch-stop. The BOX layer is then wet-etched (Fig. 1(h)). Figure 3(c) shows an optical micrograph image of the developed SON platform around an edge, where the effect of channels in venting the trapped gases is clearly visible.

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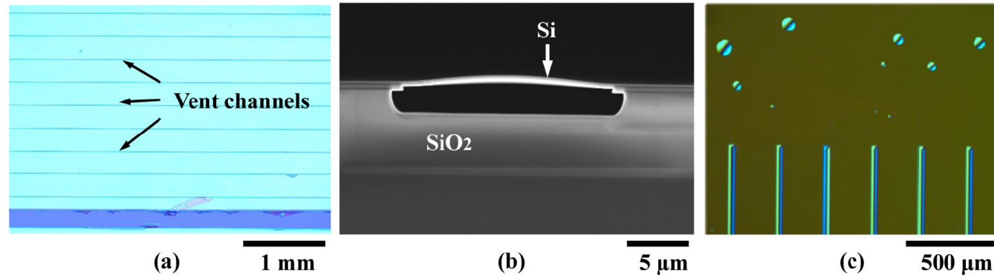

Fig. 3. (a) Top view of a void-free bonded SON piece under optical microscope. Lines represent vent channels. (b) The cross-sectional SEM of a typical vent channel after bonding process. (c) A bonded sample at the edge where the vent channels are terminated. Bubbles can be clearly seen in the area without vent channels, while the channeled area is void-free.

3. esign of the interlayer co upler

Moving forward from the single layer optical platform to hybrid platforms, it is necessary to develop a 3D integration approach for various applications. In photonic integrated circuits (PIC) implemented on hybrid coplanar material platforms, the interlayer coupler with high coupling efficiency is an essential component. Such couplers can route light among different material layers with very small loss, enabling ultra-low-insertion-loss hybrid PICs. The feasible approaches for realization of the interlayer couplers can be categorized into propagating or evanescent field coupling. In the propagating field coupling, the optical power is transferred via a propagating mode. In this category, one method involves the use of reflective surfaces to deflect light beams out-of-plane for chip-to-chip light coupling, which can be tailored to be used for intra-chip layer-to-layer light coupling. Micro-mirrors are fabricated by laser ablation [23], mechanical milling [24], or wet etching [25, 26], and waveguide-to-waveguide coupling losses as low as 2.5 dB are achieved in silicon-on-insulator (SOI) ridge waveguides using wet-etched and aluminum-coated 54.7° mirrors [26]. While the mirror-based method can offer wide operation bandwidth, the coupling loss due to the mirror surface absorption and roughness is relatively high, and the fabrication processes involved are rather complex, especially for interlayer coupling at the chip-scale. Alternatively, a pair of diffractive gratings at the two layers can be used for efficient coupling. The optimal design and fabrication of on-chip gratings have been extensively studied in recent years, especially to demonstrate efficient fiber-to-chip interconnection [27–30]. For a grating design, the best reported insertion loss (IL) is around 0.62 dB with 1-dB bandwidth of ~40 nm [29], and the highest reported 1-dB bandwidth (80 nm) has 1.3 dB IL [30]. The low IL grating includes reflective mirrors, and the high-bandwidth design utilizes a dual-level grating, which makes both approaches difficult to implement in the intra-chip coupler applications. Recently, an intra-chip diffractive grating coupler design with the back reflector has reported 1.94 dB IL and a 3-dB bandwidth of 40 nm [31]. However, the average loss of 1 dB per transition with an average bandwidth of 50 nm would limit the range of achievable on-chip functionalities in hybrid devices, where the light may transition between layers several times. A better engineering solution is needed.

To achieve higher efficiency couplers, the evanescent field coupling is a promising approach, which resorts to the decaying tail of optical modes to transport power from one waveguide to another. The utilization of the confined modes in the evanescent field coupling can inherently reduce the radiation loss compared to the propagating field coupling method. For a pair of phase-matched waveguides, it is possible to transfer all the power from one waveguide to another at a certain length at a given wavelength [32]. However, such couplers are very sensitive to the device geometry. The intrinsic wavelength dependence of the coupling efficiency (imposed by the fixed coupler length) limits the bandwidth of such couplers. To resolve this issues, inverse tapering of optical waveguides in the coupling zone has been proposed, and IL's as low as 0.2 dB, 0.4 dB and 0.06 dB in the two-layer Si platform

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[33], the Si-on-SiN platform [14], and the deposited SiN-on-Si platform [34], respectively, have been reported. However, the 3-dB bandwidth of the reported coupler in the hybrid Si-on-SiN platform in [14] is limited to 20 nm, and the demonstrated 100 nm bandwidth device has an IL of 0.8 dB.

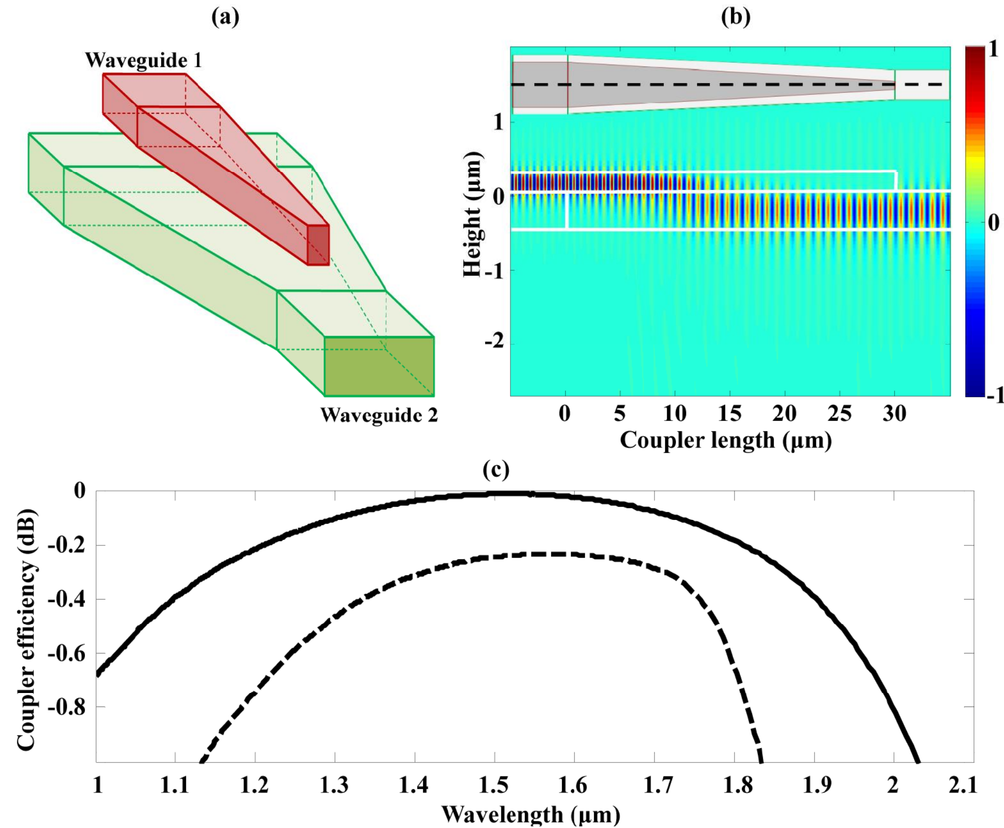

Fig. 4. (a) The schematic of the proposed coherent vertical tapering method. (b) The cross-sectional image of the electric field profile along the length of a 30-μm coherent vertical coupler; the inset is the top-view image of the coupler and the dashed line indicates the cross-section surface. (c) The computed transmission efficiency of an adiabatic interlayer coupler designed with the coherent tapering technique (solid line) compared to an efficient design of an interlayer coupler using the inverse tapering technique (dashed line). For the latter, the reported geometry in [34] is used.

To minimize the termination loss, which increases the radiation and scattering losses, we eliminate a deep sub-micron taper end using a new tapering technique. As shown in Fig. 4(a), instead of tapering down waveguide 1 while tapering up waveguide 2, we start with a wide multimode waveguide 2 and simultaneously taper both waveguides down to the single-mode width of the waveguide 2. By careful choice of the initial and final taper widths, the coupling to higher order modes can be effectively eliminated. Using the specifications of the developed hybrid SON platform, we utilize three-dimensional FDTD simulation (using Lumerical) to compare the performance of our coherent tapering technique with that of the inverse tapering method. In our platform, the thicknesses of SiN, Si, and the interface SiO_2 layers are fixed at 400 nm, 220 nm and 60 nm, respectively. Waveguide widths of 450 nm and 1 μm are chosen for single-mode operation in Si and SiN nanowires, respectively. The lower bound on the tip of the taper is 50 nm in both Si and SiN layers for reliable fabrication considerations. The upper bound of the tapering length is fixed at 30μm to facilitate dense integration. An exhaustive search is performed within the defined parameter space to find the optimal tip

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width for each material layer. The optimal widths at the Si taper end and at the SiN taper end are found to be 160 nm and 1.4 μm, respectively. Figure 4(b) shows the longitudinal cross section of the electric field profile over the 30 μm length of the coherent taper. The computed coupling efficiency spectrum of the coherent vertical coupler is plotted in Fig. 4(c), which also includes the efficiency of an inverse taper calculated using the coupler geometry reported in [34]. As shown in Fig. 4(c), the total loss of our adiabatic coupler is less than 0.02 dB over a 135 nm telecommunication bandwidth (1450-1585 nm). Additionally, the 1-dB bandwidth of the coupler is increased to cover more than an octave in frequency which paves the path for various high-bandwidth applications, such as pulse shaping and self-referenced integrated combs.

. em onstration of hybrid optical functionality

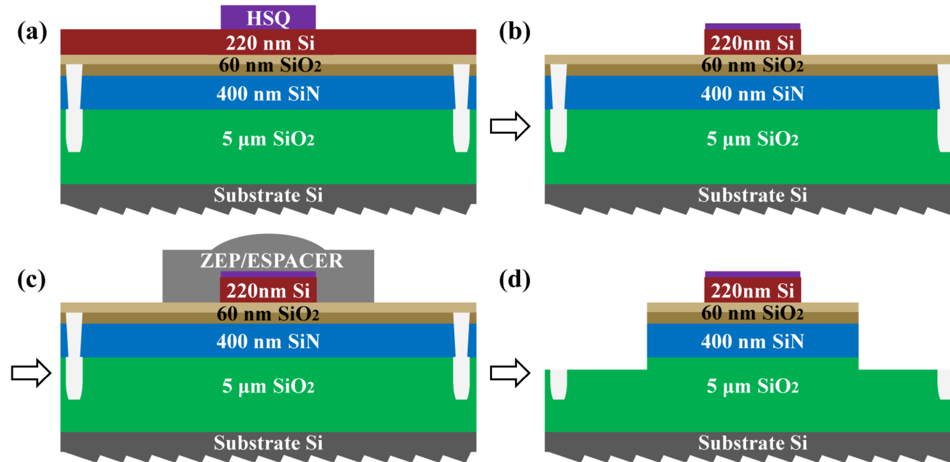

Fig. 5. A brief overview of the device fabrication process on the SON platform. (a) The first pattern is transferred to HSQ using an EBL machine. (b) The Si device layer is etched to transfer the pattern. (c) The second pattern is transferred to ZEP using the EBL machine. (d) The interface SiO_2 layer and SiN layer are etched to define the aligned second pattern on SiN.

Figure 5 outlines the device fabrication steps for implementation of the proposed interlayer coupler on the SON platform. The process begins with patterning the Si layer. The chip is spin-coated by ~150 nm of HSQ 6% (XR-1541-6 by Dow Corning), which is a negative electron-beam resist with chemical properties similar to SiO_2. As shown in Fig. 5(a), the pattern is transferred to the resist using electron beam lithography (EBL) with a JEOL JBX-9300FS system. After developing the resist in a tetramethylammonium hydroxide (TMAH) solution, an inductively coupled plasma (ICP) etching system is used to etch the Si device layer to form Si devices in a Cl_2-based plasma. The remaining residual HSQ layer is left on the Si devices (Fig. 5(b)). The SiN layer is then patterned using a second step of EBL using ZEP520A (by Zeon Chemicals) e-beam resist (Fig. 5(c)) and RIE using a fluorine (F^-)-based gas mixture (Fig. 5(d)). The residual resist is subsequently removed in piranha solution. In this process, an ESPACER (by ShowaDenko K.K.) is used on the top of ZEP resist to resolve the charge up issue.

For characterization of the fabricated devices, we use a tunable laser (Agilent 8164A) with a tunable wavelength range of 1460–1580 nm. A single-mode fiber (SMF) brings the light to the device, which is mounted on a thermally controlled stage. To control the state of polarization of the light, a 3-paddle polarization rotator is used on the input fiber. The flat-cleaved termination of the SMF delivers the optical signal to the chip, and another flat-cleaved SMF receives the light at the output. The optical signal is then collected by a detector (Thorlabs PDB150C 800–1650 nm), and the corresponding electronic signal is sampled at

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2000 samples per nm (wavelength) by a data acquisition (DAQ) board (National Instruments PCI 6259).

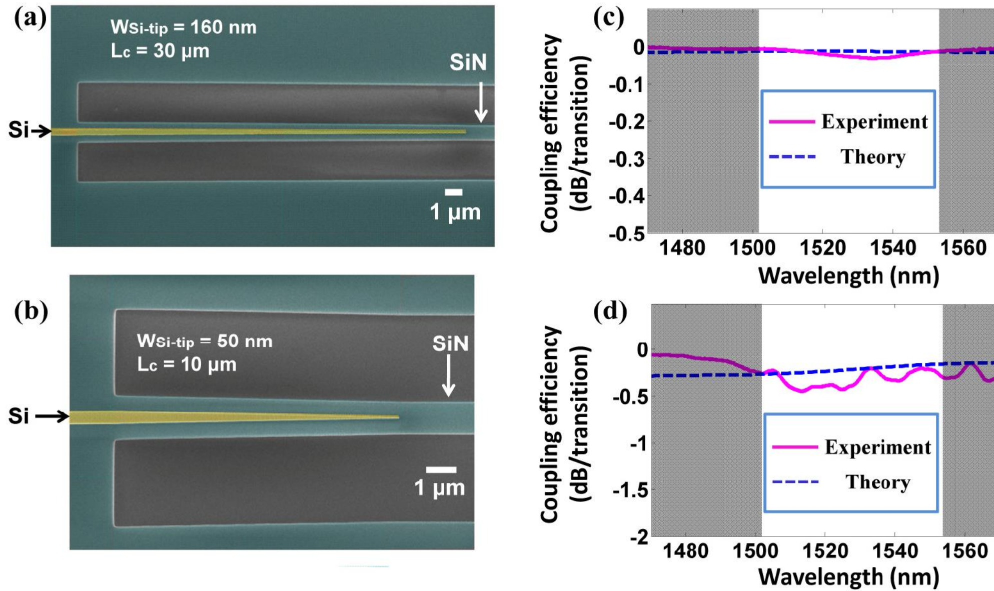

Fig. 6. (a) Colorized SEM of the adiabatic coherent vertical coupler; (b) Colorized SEM of the compact vertical coupler. (c) The experimentally measured (solid line, magenta) and theoretically calculated (dashed line, blue) spectra of the coupling efficiency of the adiabatic vertical coupler, and (d) the experimentally measured (solid line, magenta) and theoretically calculated (dashed line, blue) spectra of the coupling efficiency of the compact vertical coupler. The shaded areas in (c) and (d) mark the regions outside the bandwidth of the access input/output gratings.

In the first set of devices, two types of couplers are fabricated. The first type is the adiabatic 30 μm-long coherent vertical coupler, which is optimized for the highest coupling efficiency. The second type is the compact 10 μm-long coupler for dense integration purposes. In order to measure the coupler efficiency, we fabricate a cascaded set of 30 coherent vertical couplers with access gratings at the input and output ports. To distinguish the coupler loss from the loss due to input/output gratings as well as Si and SiN waveguide losses, a modified replica of the cascaded device is fabricated with one pair of vertical couplers. In this device, the corresponding length of the SiN and Si waveguides are chosen to be equal to the total length of the SiN and Si waveguides in the cascaded device, respectively. Using the measurement results of the replica device, the loss of 28 couplers can be isolated from all other losses of the cascaded device. Figures 6(a) and 6(b) show the scanning electron micrographs (SEM) of the fabricated adiabatic and compact vertical coupler devices, respectively. The results of characterization of the two types of couplers are shown in Figs. 6(c) and 6(d). The experimental results in each case agree well with the corresponding theoretical results as seen in the plots. The adiabatic coupler loss is experimentally extracted to be less than 0.03 dB over a wide bandwidth (1530-1565 nm), which covers the C-band. The measured loss of the compact coupler is less than 0.45 dB in the same band. The inaccuracy of the measured coupler loss is less than ± 0.01 dB, which is mainly due to the variations in fiber-to-chip coupling efficiency. The 0.03 dB loss of the adiabatic coupler in the C-band is, to the best of our knowledge, the lowest reported in any CMOS-compatible hybrid material platform. It shows that the proposed SON platform can be used for realization of practical functional integrated photonic devices with negligible loss due to multiple couplings between different material layers (i.e., Si and SiN).

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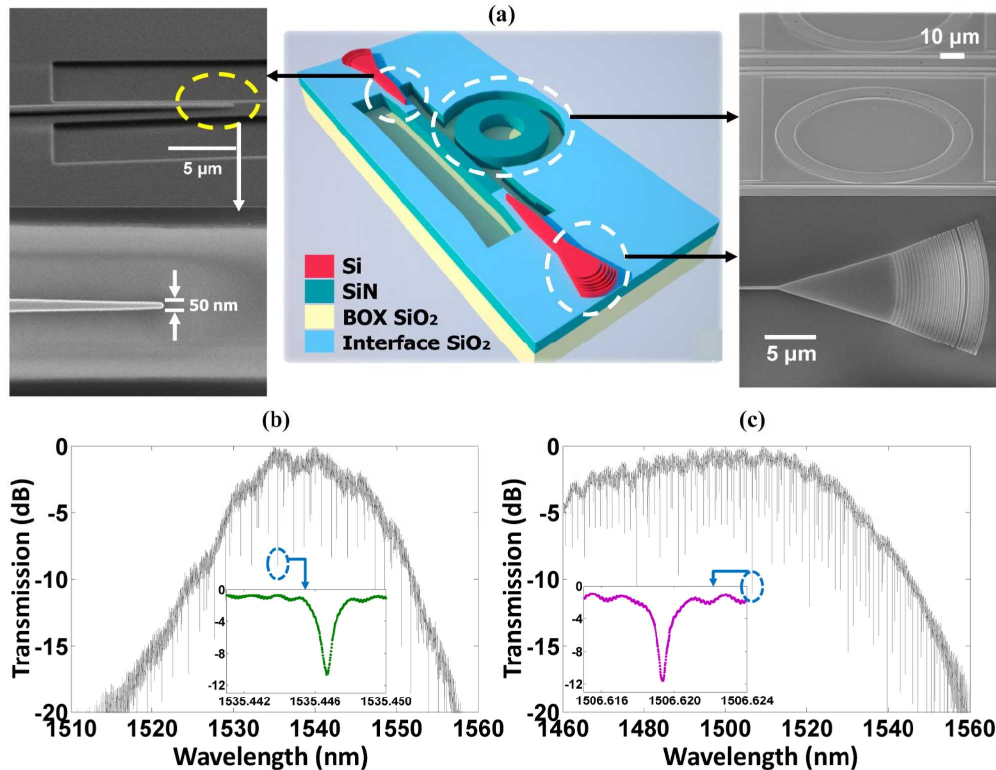

Fig. 7. (a) A schematic of the hybrid optical path with SEMs of constituent elements in the path. (b) The transmission spectrum of a 60 μm radius multimode ring resonator fabricated on the SON chip. (c) The transmission spectrum of the same SiN resonator fabricated on the inspection SiN chip. As depicted in the inset figures, the highest intrinsic quality factor in each platform is measured to be $Q_{int} \approx 3 \times 10^6$. In both of the measurements, the spectrum is limited by the input/output grating bandwidth (Si gratings in (b) and SiN gratings in (c)).

To showcase the capabilities of the proposed SON platform, we fabricated a prototype device in which a full hybrid optical path is envisaged. As shown in Fig. 7(a), the device consists of a pair of access input/output gratings (in the top Si layer) at each end, to efficiently couple light into and out of the integrated device. A pair of coherent vertical interlayer couplers at the two ends transfer the optical signal from the Si waveguide to the SiN waveguide underneath and back to the Si waveguide. The SiN waveguide is coupled (in the SiN layer) to a SiN micro-ring resonator with an outer radius of 60 μm and an inner radius of 56 μm. The gap between the SiN waveguide and the ring is ~500 nm to ensure close-to-critical coupling. Figure 7(b) shows the measured transmission spectrum of the prototype device for the TE polarization (i.e., electric field in the plane of the resonator), which is normalized by its maximum value. The characterization results show the intrinsic quality factor of the micro-resonator to be $Q_{int} = 3 \times 10^6$ in the SON platform. To draw a comparison between the quality of the low-loss layer (SiN) before and after bonding, an inspection SiN chip was prepared by cleaving a part of the piece 2 after LPCVD SiN deposition (see Fig. 1(e)). To maintain the fabrication consistency, the device fabrication on the inspection SiN chip was performed in parallel with the corresponding fabrication steps on the SON chip, as shown in Figs. 5(c) and 5(d). Figure 7(c) shows the measured transmission of a microring resonator with 60 μm radius on the SiN inspection chip. The average Q_{int} of the resonator is measured to be $\sim 3 \times 10^6$. This shows no measurable change in the quality of the low-loss SiN layer after the platform fabrication. As it has been demonstrated in [13], the quality factor of resonators can be further increased by tighter control of the (LPCVD) deposition of the SiN layer to minimize the material loss.

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The results presented in this paper demonstrate the unique functionalities of the SON platform, which can enable new capabilities using such hybrid material platform beyond those of the conventional SOI and SiN-on-SiO_2. The possibility of forming a wafer-scale material platform on which the unique advantages of Si and SiN can be combined without adding any tangible loss (either coupling or propagating losses) opens up new opportunities in forming functional devices and systems (e.g., tunable filters, transceivers, and delay lines) with considerably better performance measures compared to conventional substrates. In the SON platform, all devices with ultra-low-loss requirements (e.g., high-Q resonators, delay lines, phase shifters, etc.) can be formed in the SiN layer while all reconfigurable (or tunable) devices and mechanisms are formed in the Si layer. Additionally, SiN waveguides can be used to handle higher optical power compared to Si with minimal nonlinear effects, which can enable a novel set of tunable high power hybrid devices and systems.

5. Conclusion

We have demonstrated a new hybrid silicon-on-nitride (SON) material and device platform to enable a large range of densely integrated optical systems, with considerably better performance merits than conventional SOI or SiN-on-SiO_2 substrates. We showed a prototype hybrid device with elements of high-Q resonance and highly efficient interlayer vertical coupling, as an evidence of the unique capabilities of the proposed SON platform. For broadband adiabatic functionalities, a coherent tapered vertical coupler with record low insertion loss of 0.02 dB per transition in the IR C-band was designed and fabricated. As a part of a hybrid device, a multimode micro-ring resonator with 60 µm radius with the intrinsic quality factor of 3×10^6 was demonstrated. The inspection device test confirms no quantifiable change in the quality of the SiN layer after bonding. With the fundamental functionalities demonstrated here, the SON platform can enable the formation of practical functional integrated nanophotonic systems for a large range of applications, including optical information processing, RF photonics, and optical communication.

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